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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,801	02/18/2004	Makoto Ogawa	12377/6	9632

23838 7590 04/09/2008

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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
04/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,801	OGAWA ET AL.	
	Examiner	Art Unit	
	ROBERT E. FENNEMA	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11-25 are pending. Claims 11, 14-19, and 23 amended as per Applicant's request.

Claim Objections

1. In Claims 15 and 18, Applicant has introduced the term "the global instruction" in both Lines 3 and 4, with no antecedent basis.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 11-18 is rejected under 35 U.S.C. 102(b) as being anticipated by Rotenberg et al. (herein Rotenberg).

3. As per Claim 11, Rotenberg teaches: An information processing unit,

comprising a decoder circuit selecting an instruction group corresponding to an inputted instruction code, based on a history of the inputted instruction code, and uniquely determining an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted instruction code (Section 2.2, based on the input instruction, a trace is selected from the trace cache and output to be executed), and

wherein said decoder circuit comprises:

a code linkage part linking a group code set based on a history of the inputted instruction code with the inputted instruction code (Section 2.2, detecting a hit) , and outputting as an internal instruction code (Section 2.2, on a hit, the instructions inside the trace are output);

an internal decoder part determining an instruction to be executed in accordance with an internal instruction code to be supplied (Section 2.2 and the figure, the MUX and instruction latch use the output of the trace cache to determine which instruction to execute); and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups (Section 2.2, second paragraph, the traces) and each instruction is given with an instruction code different from others within the same instruction group in advance (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1), each instruction group having a certain instruction code to which an instruction belonging to another instruction group can be assigned (it is possible that an instruction with an address in one group will also appear in another trace, or be the target of the branch at the end of the trace, see Section 2.2, the branch fall-through and target addresses), and said decoder circuit outputting a control signal corresponding to the instruction assigned to the certain instruction code to a processor element, when said certain instruction code is inputted (Section 2.2, Second Column, Second Paragraph, upon a hit, the trace is fed to the instruction latch).

4. As per Claim 12, Rotenberg teaches: The information processing unit according to claim 11, wherein the instruction, which belongs to another instruction group and is assigned to the certain instruction code, is changeable (Section 2.2, the traces can be modified).

5. As per Claim 13, Rotenberg teaches: The information processing unit according to claim 11, wherein each of the instruction groups has a plurality of the certain instruction codes to which an instruction belonging to the other instruction group can be assigned (See Claim 11 rejection, it is possible for the same addresses to show up in other traces, especially in the partial match and multiple path alternative embodiments described in section 2.3).

6. As per Claim 14, Rotenberg teaches: An information processing unit, comprising a decoder circuit retaining information corresponding to a history of inputted instruction codes, selecting an instruction group corresponding to an inputted instruction code based on the information, and uniquely determining an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted instruction code (Section 2.2, based on the input instruction, a trace is selected from the trace cache and output to be executed), and

wherein said decoder circuit comprises:

a code linkage part linking a code concerning said information with the inputted instruction code (Section 2.2, detecting the hit), and outputting as an internal instruction code (Section 2.2, on a hit, the instructions inside the trace are output);

an internal decoder part determining an instruction to be executed in accordance with an internal instruction code to be supplied (Section 2.2 and the figure, the MUX and instruction latch use the output of the trace cache to determine which instruction to execute); and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups in advance (Section 2.2, a trace), each instruction is given with an instruction code different from other instruction codes within the same instruction group (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1), and said decoder circuit temporarily changes the information when a certain instruction code is inputted (Section 2.2, traces can be modified or replaced depending upon the input, which necessarily results in changing the data).

7. As per Claim 15, Rotenberg teaches: The information processing unit according to claim 14, wherein said decoder circuit determines an instruction to be executed, based on the inputted global instruction code only, irrespective of the information corresponding to the history of instruction codes, when the global instruction code is inputted (Section 2.2, when there is a hit, the trace is fed to the instruction latch, starting with the instruction with the same address which was input).

8. As per Claim 16, Rotenberg teaches: An information processing unit executing an instruction determined in accordance with an inputted instruction,

comprising a decoder circuit retaining information corresponding to an input history of a plurality of inputted instruction codes (Section 1.1), and uniquely determining an instruction to be executed, selected from a plurality of instructions which are assigned to the inputted instruction code in advance in accordance with a combination of the information and the inputted instruction code (Section 2.2, based on the history of a trace and the incoming address, instructions are executed).

9. As per Claim 17, Rotenberg teaches: The information processing unit according to claim 16, wherein the decoder circuit determines an instruction to be executed selected from a plurality of executable instructions (Section 2.2), and the plurality of executable instructions are sorted into a plurality of instruction groups in advance (Section 2.2, traces) and each instruction is given with an instruction code different from others within the same instruction group (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1).

10. As per Claim 18, Rotenberg teaches: The information processing unit according to claim 16, wherein said decoder circuit determines an instruction to be executed, based on the inputted global instruction code only, irrespective of the information corresponding to the history of instruction codes, when the global instruction code is

inputted (Section 2.2, when there is a hit, the trace is fed to the instruction latch, starting with the instruction with the same address which was input).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg, in view of Patterson et al. (herein Patterson).

13. As per Claim 19, Rotenberg teaches: An information processing unit,

a decoder circuit uniquely determining an instruction to be executed selected from a plurality of executable instructions based on an inputted instruction code and a group code corresponding to a history of the inputted instruction codes (Section 1.1, if a trace is encountered more than once, it is executed. The group code is the trace tag, see Section 2.2, Figure 4), and

a processor element executing an operation corresponding to a control signal provided from said decoder circuit (Figure 1), and

wherein said decoder circuit comprises:

a code linkage part linking said group code with the inputted instruction code (Section 2.2, detecting the hit), and outputting as an internal instruction code (Section 2.2, on a hit, the instructions inside the trace are output);

an internal decoder part determining an instruction to be executed in accordance with an internal instruction code to be supplied (Section 2.2 and the figure, the MUX and instruction latch use the output of the trace cache to determine which instruction to execute); and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups assigned by the group code in advance (Section 2.2, the traces) and each instruction is given with an instruction code different from others within the same instruction group (traces are made up of instructions, each with an address. See Sections 1.1 and 2.1), and the executable instruction includes an alias instruction to which an instruction belonging to the other instruction group can be assigned in advance to an internal instruction code (it is possible that an instruction with an address in one group will also appear in another trace, or be the target of the branch at the end of the trace, see Section 2.2, the branch fall-through and target addresses), but fails to explicitly teach:

comprising a plurality of processors on one chip, each processor capable of executing instructions independently.

Rotenberg teaches a superscalar machine which can execute multiple instructions in one clock cycle, but does not teach having multiple processors in this system. However, Patterson teaches that the practice of using multiple processors is

having a bigger role, due to being able to increase performance at a minimum of cost, and that the complexity of making processors more superscalar becomes a barrier (Pages 635-636). Given the advantage of increased performance for reduced cost, it would have been obvious to one of ordinary skill in the art to apply Rotenberg's invention to a machine with multiple processors, to further increase parallelism.

14. As per Claim 20, Rotenberg teaches: The information processing unit according to claim 19, wherein each of said processors further comprises a group register storing the group code, which is set up based on the history of the inputted instruction code (Section 2.2, Figure 4, the tag).

15. As per Claim 21, Rotenberg teaches: The information processing unit according to claim 20, wherein each of said processors further comprises a lookup table prescribing a change in a rule of the group code stored in said group register (Section 2.2 and Figure 4).

16. As per Claim 22, Rotenberg teaches: The information processing unit according to claim 21, wherein said lookup table is set up with a combination of an instruction mask for setting a mask bit, an instruction code for comparing the internal instruction code, and the changed group code (Section 2.2 and Figure 4).

17. As per Claim 23, Rotenberg teaches: The information processing unit according to claim 11, wherein each instruction group is given with a group code which is different than the group codes from other groups in advance, and the group code corresponding to the inputted instruction code is determined based on the history of the inputted instruction code (Section 2.2, the tag, which is unique to each group).

18. As per Claim 24, Rotenberg teaches: The information processing unit according to claim 14, wherein the information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group (Section 2.2, the tag, which is unique to each group).

19. As per Claim 25, Rotenberg teaches: The information processing unit according to claim 17, wherein the information corresponding to the history of inputted instruction codes is a group code for selected said instruction group (Section 2.2, the tag, which is unique to each group).

Response to Arguments

2. Applicant has argued that Rotenberg does not teach the claimed invention, because Rotenberg does not sort the instructions into a plurality of instruction groups in advance. However, since “in advance” has not been given a proper context, it really has no meaning until it is made clear what it is done in advance to. Is it in advance of the program running, in advance of the current instruction, in advance in the end of the

program? Until those details are put into the claim, "in advance" could mean almost anything, and as a result, Rotenberg teaches it, as Examiner can (and has) interpreted it as "in advance of the end of the program", thus whenever the cache generates the tags used to identify a cache line, it is in advance of the end of the program, since the program is running. Applicant has additionally argued that Rotenberg cannot express different kinds of instructions by one instruction code, however, this is what the trace cache does, an instruction is entered, and multiple, different instructions may come out as a result, which fits within the claim language.

3. Applicant has further argued that Rotenberg does not teach the new limitations of a decoder circuit comprising a code linkage part and an internal decoder part, and while Examiner refers the Applicant to the rejection itself for the details on why he disagrees, Examiner notes that the code linkage parts corresponds to the cache hit mechanism, where when the machine detects a hit (relating an instruction to a trace of multiple instructions), it links the instruction to the trace. As for the internal decoder part, the limitation says that the instruction code output of the linkage part is used to determine an instruction to be executed, and since the trace cache is outputting instructions to be executed, it would appear that the MUX and latch fulfill this purpose (the output will direct these units to first accept inputs from the trace cache instead of the instruction cache, then will use the instruction codes from the trace cache for the output to the system).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. FENNEMA whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Friday, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Robert E Fennema
Examiner
Art Unit 2183

RF